IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A failure analysis system, comprising:

a chip position calculation module configured to calculate fault chip positions of a plurality of circuit blocks in a chip region based on layout information on the circuit blocks positioned in the chip region and fault information on the circuit blocks;

a wafer position calculation module configured to calculate fault wafer positions in a wafer based on the fault chip positions and position information showing a chip region layout in a wafer plane; ~~and~~

a mapping module configured to perform a mapping display of the fault wafer positions in accordance with physical coordinates on the wafer plane;

an index calculation module configured to calculate a scalar quantity of a fault-extracting-index for extracting a fault mode based on a result of the mapping display; and

an index comparison module configured to compare a threshold of a the fault-extracting-index for extracting a specific fault mode to the calculated scalar quantity of the fault-extracting-index and determine the presence of the specific fault mode.

Claim 2 (Original): The system of claim 1, wherein the fault information is one of fail bit maps and pass/fail maps of the circuit blocks.

Claim 3 (Canceled).

Claim 4 (Currently Amended): The system of claim [[3]] 1, wherein the fault mode is an arc periphery fault mode.

Claim 5 (Original): The system of claim 4, wherein the arc periphery fault is biased toward a periphery region of the wafer and has a geometric symmetry.

Claim 6 (Currently Amended): The system of claim [[3]]1, further comprising a classification module configured to set a hierarchical structure between a plurality of fault-extracting-indices and performs detection and classification of unknown fault modes based on classification information in which the fault-extracting-indices are classified in the hierarchical structure.

Claim 7 (Original): The system of claim 6, wherein the hierarchical structure includes at least an arc periphery fault, a periphery fault including the arc periphery fault and a cluster fault including the periphery fault.

Claim 8 (Currently Amended): A failure analysis method, comprising:

reading out layout information on a plurality of circuit blocks disposed in a chip region, position information showing a chip region layout in a wafer plane and fault information on the circuit blocks;

calculating fault chip positions in the chip region of the circuit blocks based on the layout information and the fault information;

calculating fault wafer positions in a wafer based on the position information and the fault chip positions; ~~and~~

subjecting the fault wafer positions to a mapping display in accordance with physical coordinates on the wafer plane;

calculating a scalar quantity of a fault-extracting-index for extracting a fault mode based on a result of the mapping display; and

determining the presence of the fault mode by comparing the scalar quantity of the fault-extracting-index with a threshold stored in a threshold information storage unit.

Claim 9 (Original): The method of claim 8, wherein the fault information is one of fail bit maps and pass/fail maps of the circuit blocks.

Claim 10 (Canceled).

Claim 11 (Currently Amended): The method of claim [[10]]8 wherein the fault mode is an arc periphery fault mode.

Claim 12 (Original): The method of claim 11, wherein the fault-extracting-index is calculated by a degree of bias of fault densities in a region where the arc periphery fault occurs and by a degree of continuity of the longest continuous faults adjacent two of which is spaced apart by a distance within a threshold in the region where the arc periphery fault occurs.

Claim 13 (Currently Amended): The method of claim [[10]]8, further comprising:

setting a hierarchical structure between a plurality of fault-extracting-indices; and

performing detection and classification of unknown fault modes based on classification information in which the fault-extracting-indices are classified in the hierarchical structure, and a result of determining the presence of the fault mode for each of the fault-extracting-indices.

Claim 14 (Original): The method of claim 13, wherein the hierarchical structure includes at least an arc periphery fault, a periphery fault including the arc periphery fault and a cluster fault including the periphery fault.

Claim 15 (Original): The method of claim 13, wherein the fault mode is classified as the unknown fault mode concerning upper-level fault-extracting-index when it is determined that there is a fault in the upper-level fault-extracting-index of the hierarchical structure and there is no fault in fault-extracting-index one level lower than the upper-level fault-extracting-index.

Claim 16 (Currently Amended): A computer program product configured to be executed by a computer, comprising:

an instruction of reading out layout information on a plurality of circuit blocks disposed in a chip region, position information showing a chip region layout in a wafer plane and fault information on the circuit blocks;

an instruction of calculating fault chip positions in a chip region of the circuit blocks based on the layout information and the fault information;

an instruction of calculating fault wafer positions in a wafer based on the position information and the fault chip positions; ~~and~~

an instruction of subjecting the fault wafer positions to a mapping display in accordance with physical coordinates on the wafer plane;

an instruction of calculating a scalar quantity of a fault-extracting-index for extracting a fault mode based on a result of the mapping display; and

an instruction of determining the presence of the fault mode by comparing the scalar quantity of the fault-extracting-index with a threshold stored in a threshold information storage unit.

Claim 17 (Withdrawn): A manufacturing method for a semiconductor device, comprising:

fabricating a plurality of integrated circuits on a wafer, by assigning a plurality of chip regions for each of the integrated circuits such that each of the chip regions has a plurality of circuit blocks disposed therein, by sequentially executing a plurality of manufacturing processes;

obtaining fault information by measuring characteristics of the circuit blocks, respectively;

detecting a fault based on a result of a mapping display performed for the fault information in accordance with physical coordinates on a wafer plane by use of layout information on the circuit blocks disposed in the chip region; and

performing at least one of a repair of a manufacturing apparatus used for the manufacturing, a remodeling of the manufacturing apparatus, and a modification of a recipe of a specific manufacturing process in the plurality of manufacturing processes causing the fault to occur.

Claim 18 (Withdrawn): The method of claim 17, wherein the fault information is one of fail bit maps and pass/fail maps of the circuit blocks.

Claim 19 (Withdrawn): The method of claim 17, wherein the detection of the fault comprises:

calculating fault-extracting-index of a fault mode based on the result of the mapping display; and

determining the presence of the fault mode by comparing the fault-extracting-index with a threshold stored in a threshold information storage unit.

Claim 20 (Withdrawn): The method of claim 19, wherein the fault mode is an arc periphery fault.

Claim 21 (Withdrawn): The method of claim 20, wherein the fault-extracting-index is calculated by a degree of bias of fault densities in a region where the arc periphery fault occurs and by a degree of continuity of the longest continuous faults adjacent two which is spaced apart by a distance within a threshold in the region where the arc periphery fault occurs.

Claim 22 (Withdrawn): The method of claim 19, wherein the detection of the fault further comprises:

setting a hierarchical structure between a plurality of fault-extracting-indices; and

performing detection and classification of unknown fault modes based on classification information in which the fault-extracting-indices are classified in the hierarchical structure, and a result of determining the presence of the fault mode for each of the fault-extracting-indices.

Claim 23 (Withdrawn): The method of claim 22, wherein the hierarchical structure includes at least an arc periphery fault, a periphery fault including the arc periphery fault and a cluster fault including the periphery fault.

Claim 24 (Withdrawn): The method of claim 22, wherein the fault mode is classified as the unknown fault mode concerning upper-level fault-extracting-index when it is determined that there is a fault in the upper-level fault-extracting-index of the hierarchical structure and there is no fault in fault-extracting-index one level lower than the upper-level fault-extracting-index.